REMARKS

The Office Action dated June 2, 2005 has been received and reviewed. Claims 1-7, 12-17 and 22-26 stand rejected. Applicants gratefully acknowledge the allowability of dependent claims 8-11, 18-21 and 27. Claims 1, 23 and 24 are currently amended by this response, and new claim 28 is added. Accordingly, claims 1-28 are presently in the application.

New claim 28 is a combination of rejected claim 24 and allowable dependent claim 27, which depended directly from claim 24; new claim 28 should therefore be allowable as it stands.

A. The Yasuda reference and its application to the claims.

Claims 1-3, 13, and 23-26 stand rejected under 35 USC 103(a) as being unpatentable over Yasuda (US 6,081,347). Referring to Figure 2 of the Yasuda patent, and as referenced in the present rejection, Yasuda discloses a high-speed CPU bus 204 for transferring data by establishing mutual connection between a CPU 201 which performs the "whole control", a large capacity hard disc drive (HDD) 202 which is controlled by the CPU 201 to contain a plurality of applications to be executed by the CPU 201, and a raster image processor (RIP) 205 which receives, via the high speed CPU bus 204, an image formation command. The HDD is also used to temporarily store image data on demand. The high speed CPU bus 216 is controlled by the CPU 201 as a singular component to transfer data among the various other components. It is noteworthy that only one bus is disclosed for these purposes, operating according to some predetermined high speed bus protocol.

In rejecting claims 1-3, 13 and 23-26, and in comparing Yasuda to the claims in the application, the Examiner argues that Yasuda discloses an image processor comprising a first processor system (201) having a first bus for communication with the image source 202 and a second processor system (205) in circuit communication with the first processor system (201) and having a second bus for communication with the image source 202. The bus in both cases is described, respectively, as the bus connecting the first processor system (201) to HDD (image source) 202, and the second processor system (205) to HDD 202. Yasuda however clearly shows one and the same bus connecting the first

processor system (CPU 201) and the second processing system (RIP 205) to HDD 202, namely, the high speed CPU bus 204 (col. 4, lines 43-64).

In other words, and for sake of argument, if the high speed CPU bus 204 is considered to be the "first bus" connecting the first processor (201) to the image source 202, there is nothing in Yasuda showing any suggestion of a "second bus" for connecting the second processor (205) to the image source 202. Nor is there any need for providing a second bus in this situation, *that is separate and distinct from the first bus*, inasmuch as both processing units (201) and (205) require and use the same high speed CPU bus configuration for interconnecting with the HDD (image source) 202, that is, the high speed CPU bus 204. Absent such need, any motivation for adding a second bus to connect the second processor (205) with the image source 202, particularly one operating *according to a second bus protocol that is different than the first bus protocol for the high speed CPU bus,* is completely missing.

B. The Invention According to Amended Claim 1.

In contrast with Yasuda, the system according to the present invention (as shown in Figure 2 of the specification) includes an image processor 14 having a printer image data path that is separate from its printer control and status path. More specifically, the image processor 14 comprises a first processor system 30 and a second processor system 32 separately connected to an image source 12. The first processor system 30 is characterized by providing high-level control of the image processing performed within the image processor 14. The first processor system 30 also provides high-level control of image acquisition performed by the image processor 14, e.g., handshaking during image transfers from the image source 12 to the second processor system 32. Thus, the first processor system 30 coordinates or orchestrates control of image acquisition. The second processor system 32 is characterized by performing a majority of the image processing performed within the image processor 14 responsive to control by the first processor system 30. Furthermore, the second processor system 32 accepts and stores images from the image source 12, as coordinated by the first processor system 30 via a control/status bus 42.

More specifically, the first processor system 30 is in circuit communication with the image source 12 via *a first bus*, referred to as a print

control bus 34. The second processor system 32 is in circuit communication with the image source 12 via *a second bus*, referred to as an image data bus 36, that is separate and distinct from the first bus. The advantage of the invention is that the separate processors and *separate bus paths* for printer image data and printer control and status data allow the system to minimize the "housekeeping" performed by the processor system performing the image processing, thereby streamlining image processing and increasing the speed of high-speed printing.

In claiming an image processor for generating image output for a printer from image data received from an image source, amended claim 1 therefore recites two processor components and two bus configurations: (a) a first processor system, characterized by having *a first bus for communication with the image source*, where the first processor system communicates control data with the image source via the first bus... ; and (b) a second processor system in circuit communication with the first processor system and characterized by having *a second bus for communication with the same image source that is separate and distinct from the first bus*, where the second processor system receives image data from the image source via the second bus (italics added for purpose of these remarks).

C. The Invention According to Amended Claim 23 and 24.

Furthermore, the first bus, the print control bus 34, can be a bus of virtually any protocol; however, since speed of transfer is not critical for the print control bus 34, a slower bus protocol may be used. The processor system 32 is in circuit communication with the image source 12 via the second bus, referred to as the image data bus 36. Although virtually any bus protocol can be used for the image data bus 36, because image files can be very large, speed of transfer is important between the image source 12 and the second processor system 32 along that bus. Therefore, any of a number of known faster bus protocols are preferred for the image data bus 36 (see page 8, lines 12-27 of the specification).

Consequently, in claiming an image processor for generating image output for a printer from image data received from an image source, amended claim 24 therefore recites two processor components and two bus protocol configurations: (a) a first processor system, characterized by having a print control bus providing a printer control and status path for communication

with the image source *according to a first bus protocol*, where the first processor system communicates control data with the image source via the print control bus... ; and (b) a second processor system in circuit communication with the first processor system and characterized by having an image data bus providing a printer image data path separate from said printer control and status path for communication with the image source *according to a second bus protocol that is different than the first bus protocol*, where the second processor system receives image data from the image source via the image data bus (italics added for purpose of these remarks). Independent claim 23 has similar limitations.

D. The Obviousness Rejections.

It is respectfully suggested that a rejection under 35USC103(a) may not be maintained unless, among other requirements, (1) all of the claim limitations are taught or suggested by the prior art, and (2) there is some suggestion or motivation in the first place to draw upon the cited prior art, such that each claim limitation is taught or suggested in the prior art. These are among the requirements for a *prima facie* case of obviousness. MPEP 2143.01 – 2143.03. Yasuda fails to show any suggestion or motivation for minimizing the "housekeeping" performed by the processor system by enhancing the disclosed bus with the connection of an additional bus to the same image source for providing data transfer, and furthermore with the connection of the additional bus to the same image source for providing data transfer according to a separate protocol. Accordingly, pending claims 1-3, 13 and 23-26, as amended, are believed to be unobvious over Yasuda, and allowable as now presented.

Claims 4-7, 12, 14-17 and 22 stand rejected under 35 USC 103(a) as being unpatentable over Yasuda as applied to claims 1-3 and further in view of Clark (US 5,899,604). Claim 4-7 and 12 are dependent on claim 1 and claims 14-17 and 22 are dependent on claim 24, and therefore include all the features thereof. Accordingly, for the reasons set forth above with regard to claims 1 and 24, claims 4-7, 12, 14-17 and 22 are also believed to be patentable.

The remaining reference – Menendez et al (US Patent No. 5,113,494) – was not relied upon by the Examiner on its merits in relation to the claims but merely considered pertinent to applicant's disclosure. It has been

considered for purposes of this response but is at most cumulative and not believed to be otherwise relevant.

It is believed that these changes now make the claims clear and definite and, if there are any problems with these changes, Applicants' attorney would appreciate a telephone call.

In view of the foregoing, it is believed none of the references, taken singly or in combination, disclose the claimed invention. Accordingly, this application is believed to be in condition for allowance, the notice of which is respectfully requested.

Respectfully submitted,

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If the Examiner is unable to reach the Applicant(s) Attorney at the telephone number provided, the Examiner is requested to communicate with Eastman Kodak Company Patent Operations at (585) 477-4656.